GPS Disciplined
10 MHz Frequency Standard

by

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Contents

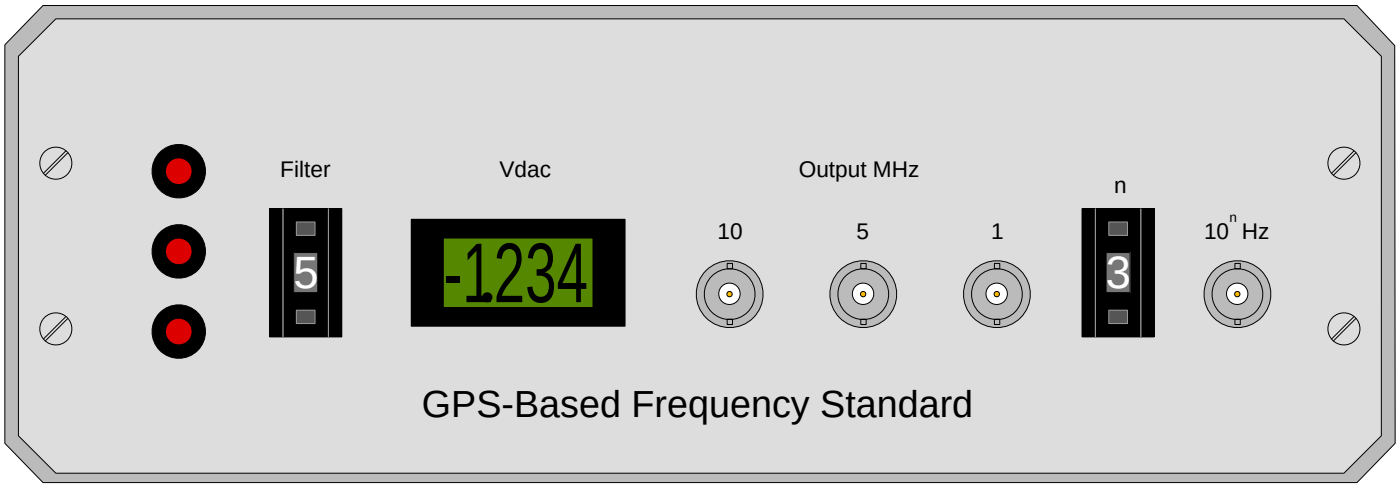
1. Description

This frequency standard is based on a *Hewlett Packard* double-oven HP 10811 crystal oscillator [5] maintained by the 1 pulse-per-second signal from a *Rockwell/Conexant/Navman* Jupiter-T GPS receiver [1]. Short term frequency accuracy is of order 1 part in 10^{11} ; day to day accuracy is of order 1 part in 10^{13}, and very long term accuracy matches that of the GPS system itself.

The PIC-based microcontroller and related logic that interfaces GPS 1PPS and 10 MHz oscillator, was designed by *Brooks Shera*, published in QST Magazine [2] and Internet [3].

Output frequencies are 10 MHz, 5 MHz and 1 MHz, plus selectable 1 Hz-100 kHz in decade steps to front panel BNC sockets.

Front Panel



2. Operation

Connect to 230V ac mains electricity using a grounded outlet, and a cable with a 3-pole IEC connector at the equipment end. The equipment fuse is rated 500mA. Power consumption is about 40W from cold, 15W when stabilised.

A GPS antenna should be connected to the MCX female socket on the rear panel. This socket has 5V available, at up to 80 mA to power an active antenna. The receiver should lock onto the GPS satellites within 2 minutes from cold, or only a few seconds if warm.

The HP10811 inner oven takes about 5 minutes to warm up, and its outer oven up to 60 minutes.

The left-hand numeric push-button switch "Filter" should be set to value 1, and the LCD digital voltmeter reading will stabilise when preliminary system lock is achieved. This will take up to 15 minutes from cold, less if already warm.

When stabilised, the Filter control can gradually be increased to 5 or 6. The system characteristic time constant is 1500s at setting 2, doubling for each increase, up to 13 hours. Settling time is commensurate with these periods, typically 5 hours from a cold start with N=5.

HCMOS signals at frequencies of 10 MHz, 5 MHz and 1 MHz are available from the three central BNC sockets, whilst the right-hand numeric push-button switch selects from 1 Hz to 100 kHz in decade steps ("0" = 1 Hz) and outputs to the fourth BNC socket.

GPS and Controller Diagnostic Data is available in RS-232 format at DE-9S sockets on the rear panel.

You can also use the oscillator without GPS signals. The Filter control must be set to "0" and the system should be allowed to warm up for at least 10 minutes. Performance will then follow basic HP10811 specifications [4] and frequency accuracy is typically well within 0.05 Hz, depending on aging since last calibration (see Adjustments).

3. Equipment Modules

3.1 Oscillator [4,5]

The 10 MHz double-ovened oscillator HP10811-60158 was obtained, together with its PSU, from a surplus *HP Z3801A GPS Receiver* time and frequency standard. These units were used in USA cellular telephone base stations during the mid to late 1990s, and appeared on the market in large numbers after about 5 years operation.

It has three parts; the oscillator, inner oven and outer oven. These parts are electrically independent.

The oscillator and inner oven are essentially as per the HP10811D/E product, except that the EFC is 10x more sensitive, -1.00 Hz/volt. The output is a 2.5V pk-pk (0.9V rms) sine wave when loaded with 250 ohm. The oscillator runs on regulated 12V and consumes 25mA when fully warmed.

The inner oven requires 12-30V; 24V is used here, and uses 380mA when cold, 60mA when hot and 25 mA when the outer oven is hot.

The outer oven behaves as an 18 ohm resistor, and requires between 4W and 10W of heat. Control of this power is done by DC-DC conversion and power amplifier circuitry on the associated power supply PCB.

3.2 GPS Receiver [1]

The GPS engine used is a *Navman* (formerly *Rockwell* and *Conexant*) 'Jupiter-T', part TU60-D120-041. This is a 12 parallel channel engine, with a CPU rate around 45 MHz, so the 1 PPS output pulses have ~25 ns granularity. The receiver is optimised for static time/frequency applications. The command

interface is compatible with *Motorola* UT+ "@@" protocols, as well as having a native *Rockwell* binary mode and *NMEA* plaintext outputs. The engine can be left to perform as given at start-up, and optionally can be tuned by via software commands.

3.3 'Shera' System Controller [2]

The function of this controller is to take 1 PPS pulses from the GPS engine, and generate an EFC voltage to control the oscillator frequency. Additional features (such as LEDs etc) on front and rear panels are also serviced. The controller PCB [6] is modified slightly as follows:

- A second 74HC4520 is piggy-backed to U2 as described in [3] to increase the division ratio to 32, which is better matched to a 10 MHz oscillator.
- DIP switches S1/2/3, which set the control filter time constant, have been brought out to a front panel thumbwheel switch via connector P5 by paralleling S1/2/3 with S6/7/8. Those six switches are therefore unused and must be set open circuit (off).
- A multi-turn trimpot has been added to the PCB in order to fine adjust the static EFC voltage (needs about -0.8V) and to set the frequency sensitivity to 7.5 x 10^{-9} per DAC volt, the value required by the design.
- A 1s time constant RC reset circuit is added for the PIC U8. (Pin 1 is now isolated from direct +5V).

3.4 Power Supply

This comprises a) 230Vac mains power supply, b) DC-DC PSU board and c) three power regulator ICs.

Mains supply

The mains supply generates 54V DC (max 750mA) via a simple 36Vac/50VA transformer, bridge rectifier and 4700µF capacitor.

PSU Board

The main power conditioner, originally part of the *HP* Z3801A unit, accepts 54V DC input and generates +5V, +15V and -15V for off-board equipment, and an on-board +5V supply for the outer oven controller. A 2200µF 40V capacitor has been added to bridge the +15V and -15V outputs. This is to suppress an LF relaxation mode oscillation on the +/-15V supplies caused by the high start-up current surge from the inner oven.

A 10k resistor bridges PCB connector P2 pins 1 and 8. This pulls pin 8 high for outer oven always ON.

Regulators

An LM7812 is used to provide stabilised 12V for the oscillator, and an LM7812/7912 pair stabilises +/-12V supplies to the inner oven. These three regulators are bolted to the chassis floor. Total dissipation is initially 2.3W falling to 300mW once the inner oven is warm.

Power Consumption

54V Supply (typ)

Start up	50.0V @ 750 mA	= 38W
Steady state	55.2V @ 270 mA	= 15W

15/-15/5V Supplies

10 MHz oscillator	12V 25 mA	
Inner oven cold (outer hot)	24V 380 mA	(+12V and -12V in series)
Inner oven hot (outer hot)	24V 25 mA	
'Shera' Controller	5V 65 mA	and -5V 10 mA
Panel meter	5V 40 mA	(backlight on)
GPS Engine	5V 195 mA	
Antenna	5V 25 mA	
Divider logic	5V 15 mA	

3.5 Divider Logic

The logic unit takes a 2V pk-pk 10 MHz sinewave input and outputs decade 1 Hz to 10 MHz, and 5 MHz HCMOS (TTL level) signals.

74AC14 U1 is a fast hex inverter with Schmidt trigger inputs that serves a) as an input buffer and b) as output drivers to the 10/5/1 MHz front panel BNC sockets. 74HC14 U6 buffers outputs at the six lower frequencies

The 74HC390s U2-5 are a dual divide by 10 counters. Each consists of a divide by 5 (which has an asymmetric output), and a divide by 2. U2a is used for 5 MHz; all other sections are used as divide by 10.

4. Adjustments

The only adjustment available is to set the EFC static voltage. This might be required if ageing or component drift has resulted in an ADC output voltage near the end of its range of ±3V. The present ADC output voltage can be read on the LCD panel meter (range ±1.999 V).

To reset the EFC static voltage:

1. Connect a DVM (digital voltmeter) to the EFC line at controller P8 pin 3 and pin 4 (gnd) or similar.
2. When the system is fully locked up and stable, write down the EFC voltage.
3. Set the filter switch to N=0, (set-up mode) which puts the DAC output close to 0V. Wait 30s for the controller to recognise the change.
4. Adjust the trimpot until the DVM reading is identical to that recorded at step 2.
5. Restore the filter switch setting as per normal start-up procedure.

5. Components

Panel meter: *Lascar*

DPM 3AS-BL 3.5 digit backlit LCD voltmeter module

Switches: *Cherry PE series*

BCD+complement	UPEFA3000
Decimal	UPEAA3000
LH end cheek	6090754
RH end cheek	6099756
Stop pin(s)	6070013

MCX Connectors: *Huber+Suhner*

Panel female crimp, for RG178 24MCX-50-1-13/111NH

Straight male crimp, for RG178 11MCX-50-1-13/111NH

Enclosure: *OKW Enclosures Ltd (UK)*

Unicase 2, part number M5502110 90h x 260w x 250d `http://www.okw.co.uk/`

References

1. Jupiter-T Data Sheet
`http://www.jrmiller.online/projects/docs/10039C.PDF`

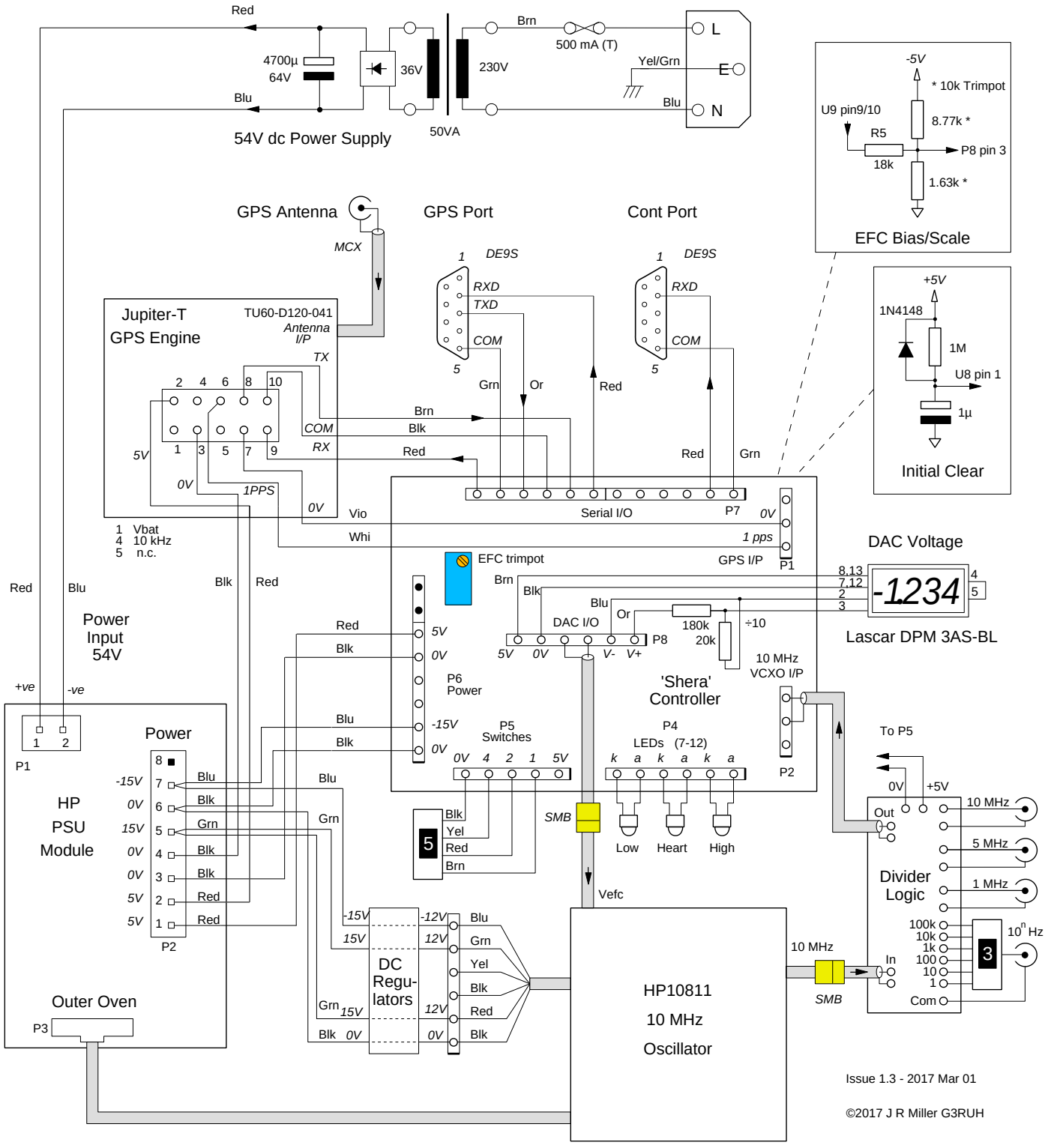
2. *A GPS-Based Frequency Standard*, by Brooks Shera W5OJM, QST 1998 July, ARRL. Pages 37-44.

3. Additional information about the controller including .PDF file of the article [2]
`https://web.archive.org/web/20171229173858/http://www.rt66.com/~shera/index_fs.htm`

4. HP10811D/E Catalogue Data Sheet scan
`http://cp.literature.agilent.com/litweb/pdf/5091-1639E.pdf`

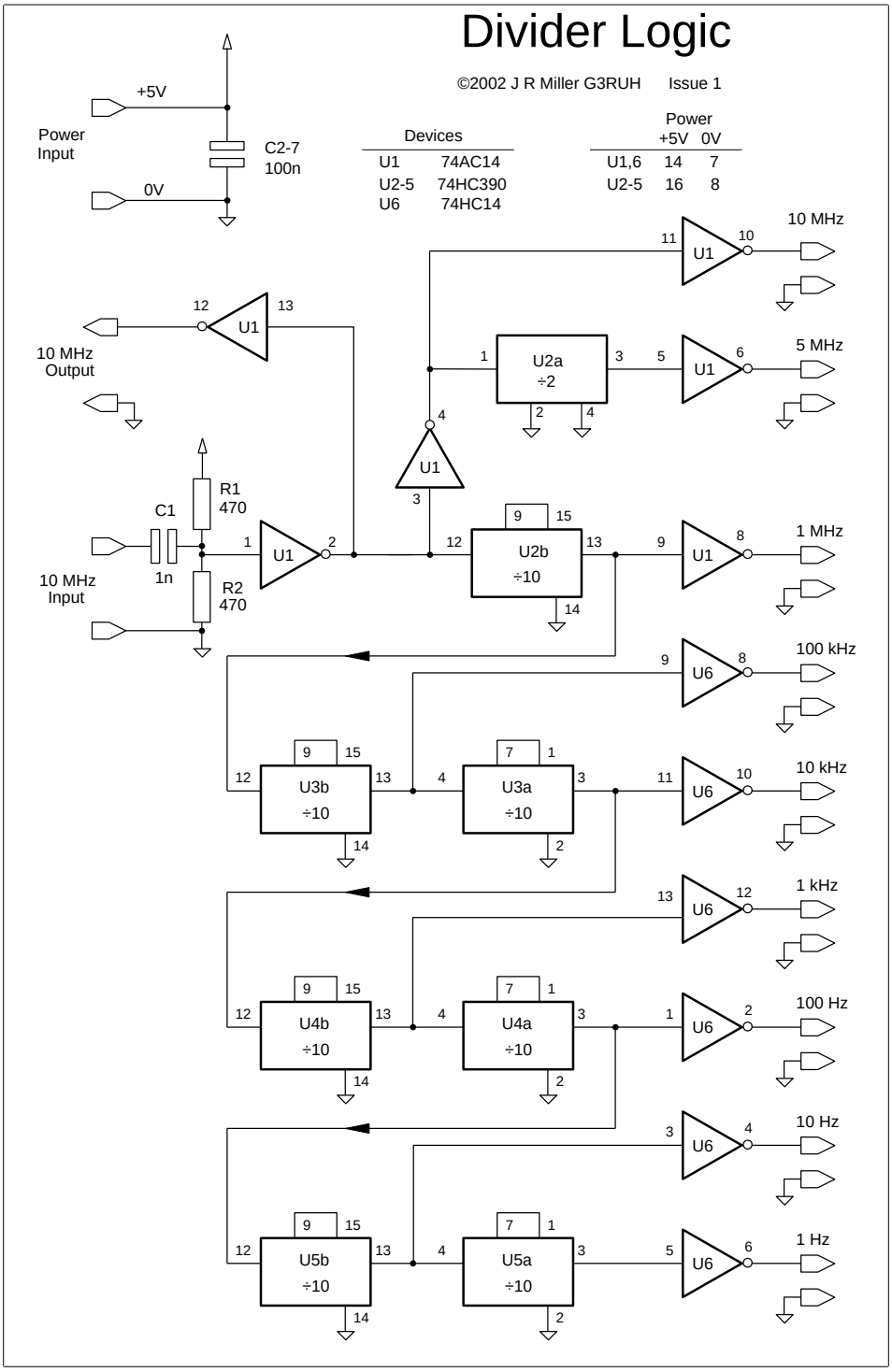
5. HP10811D/E Performance Specifications
`http://www.febo.com/pages/hp10811/HP10811-Specs.pdf`

6. Controller PCB source: `http://a-aengineering.com/`

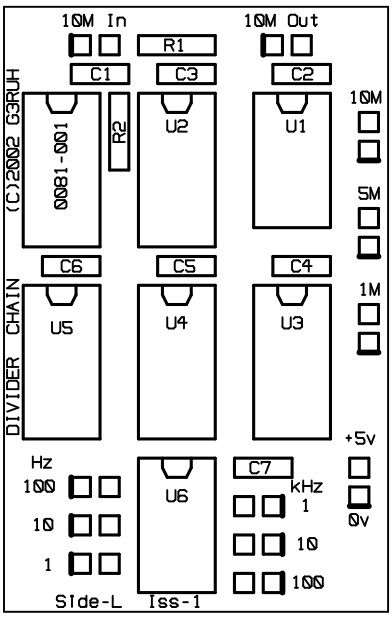


GPS Disciplined 10 MHz Oscillator

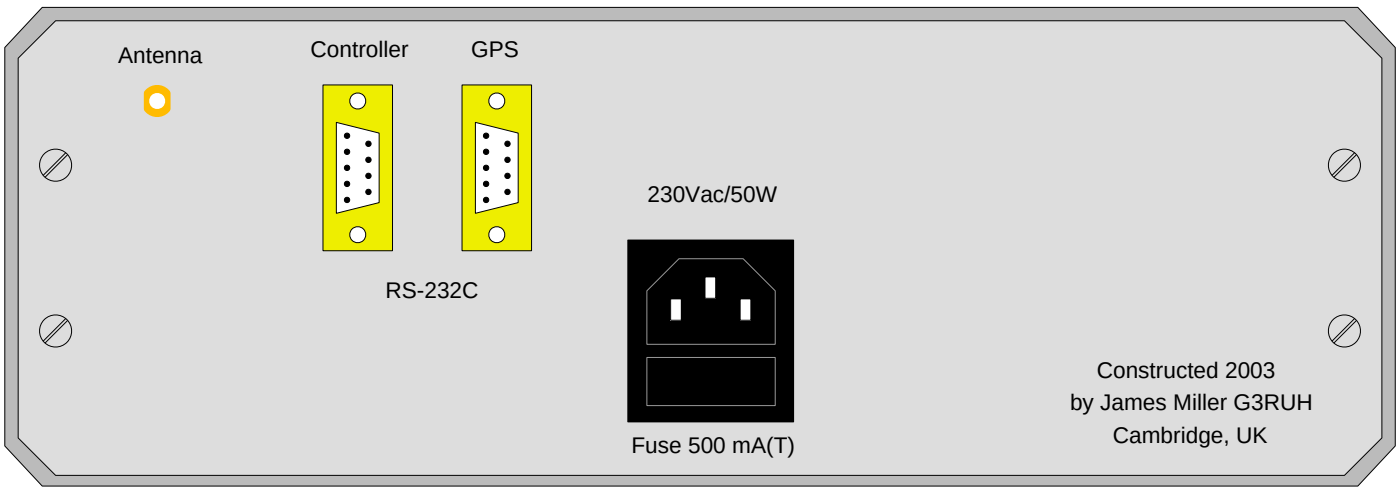
Divider Logic



Divider PCB Layout



Rear Panel



Performance Specifications for HP 10811-60158 Crystal Oscillator [5]

Source: HP Dwg.No. A-10811-90027-1 rev.H 1999-Oct-26

1 Output Signal

Frequency: 10.000000 MHz.
Voltage: 0.55V ± 50mV rms into 50 ohm.
Harmonic Distortion: < -25 dBc.
Spurious Phase Modulation: < -100 dBc (discrete sidebands 10 Hz to 25 kHz).

2 Frequency Adjustment

Coarse Tuning Range: > ± 5×10^{-7} (± 5 Hz).
Electronic Frequency Control (EFC): > ± 2×10^{-7} (± 2.5 Hz) for control range of -5V to +5V

3 Frequency Stability

Long Term Stability (Aging Rate):
< 2.5×10^{-10} / day after 24 hour warm up when:
oscillator off time was less than 24 hours and
oscillator aging rate was < 2.5×10^{-10} / day prior to turn off.
< 2.5×10^{-10} / day in less than 30 days of continuous operation
for off time of greater than 24 hours.
< 1×10^{-7} / year for continuous operation
(Typical 1×10^{-8} / year after 1 year)

Aging rate (long term frequency stability) is defined as the absolute value (magnitude) of the fractional frequency change with time. An observation time sufficiently long to reduce the effects of random noise to an insignificant value is implied. Frequency changes due to environmental effects must be considered separately.

4 Time Domain Stability:

Averaging Time seconds	Stability $\sigma_y(\tau)$
.001	< 1.5×10^{-10}
.01	< 1.5×10^{-11}
.1	< 5.0×10^{-12}
1	< 9.8×10^{-13}
10	< 5.0×10^{-12}
100	< 1.0×10^{-11}
(Typical)1000	< 1.0×10^{-11}

Time domain stability $\sigma_y(\tau)$ is defined as the two sample deviation of fractional fluctuations due to random noise in the oscillator. The measurement bandwidth is 100 kHz. See NBS Monograph 140 for measurement details.

5 Frequency Domain Stability (Phase Noise):

Offset from Signal Hz	Phase Noise dBc
1	< -95
10	< -125
100	< -135
1000	< -145
10000	< -150

Frequency domain stability is defined as the single sideband noise to signal ratio per Hertz of bandwidth (a power spectral density). This ratio is analogous to a spectrum analyzer display of the carrier versus either phase modulation sideband. See NBS Monograph 140 for measurement details.

6 Warm Up

< 5×10^{-9} of final value 10 minutes after turn on when: a) oscillator is operated in a 25° C environment with 20 Vdc oven supply voltage; b) oscillator off time was less than 24 hours; c) oscillator aging rate was < 5×10^{-10} / day prior to turn off; d) Final value is defined as oscillator frequency 24 hours after turn on.

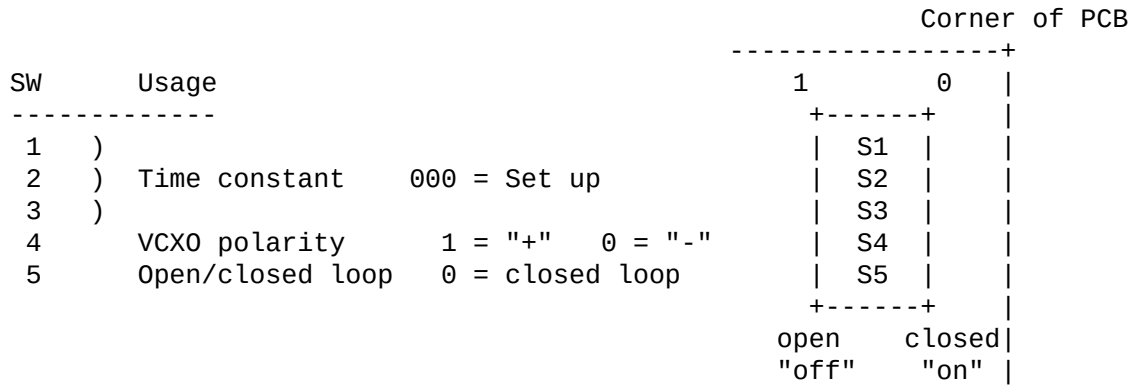
7 Environmental Sensitivity

7.1 Temperature
Frequency Change: < 4.5×10^{-9} from 0° C to +71°C.
Operating Range: 0° C to +71°C.
Storage Range: -55° C to +85°C.
7.2 Load: < 5×10^{-10} for ± 10% change in 50 ohm load on output.
7.3 Power Supply
Oscillator Supply: < 2×10^{-10} for 1% change.
Oven Supply: < 2.5×10^{-10} (< 1×10^{-10} typical) for 10% change.
7.4 Gravitational Field: Not specified
7.5 Magnetic Field: Sidebands < -90 dBc for 0.1 mT (1 Gauss) field at 100 Hz
7.6 Humidity (typical): < 1×10^{-9} for 95% relative humidity at 40° C.
7.7 Shock (survival): 30 g, 11 ms, ½ sinewave.
7.8 Altitude (typical): < 2×10^{-9} for 0 to 50,000 ft.

8 Power Requirements

8.1 Oscillator Circuit: 11.0 to 13.5 Vdc. 30 mA typical, 40 mA. < 100 µV ripple and noise
8.2 Inner Oven Circuit: 12 to 30 Vdc, 11 W max at turn on.
Steady state power drops to approximately 2 W at 25° C in still air at 20 V.

DIP Switch Settings
These paragraphs are extracted from [2,3].



Set Up Mode
S1/2/3 all closed (N=0) is setup mode. The controller's High and Low LEDs indicate when the frequency is too high or too low.

N=1 and above: the High LED indicates that the phase is far from the set point (800), suggesting that the phase lock is questionable.

When N=4,5,6,7 the Low LED shows when the de-glitcher algorithm (see footnote 10 in the article) is operating to delete a spurious phase reading.

Time Constants
The software provides six different filter time constants, ranging from no filtering at all, to a time constant of many hours. The time constant, which is chosen by setting S1/2/3, can be changed on the fly while the controller is running.

Switches S1/2/3 can be considered as controlling a 3-bit number N in the range 0 to 7 where closed is 0 and open is 1. Then, N=0 is setup mode, N=1 implements a first order PLL with no filtering beyond the 30 second integration of the phase measuring circuit, and N=2 to 7 implement second order PLLs with time constants T starting at 1500 seconds and increasing by a factor of two at each step to approximately 13 hours. Here $T = 2\pi/\omega_n$ where ω_n is the natural loop frequency. It is approximately the time required for the PLL to recover from a transient.

VCXO Polarity
If the VCXO frequency increases when the control voltage is increased, open S4. If the frequency decreases with increasing voltage, close S4.

Open/Closed Loop
Opening S5 will hold the DAC voltage at its current setting, thereby preventing the controller from further changing the VCXO frequency. In normal operation S5 should be closed, but opening it for short periods is an effective method of eliminating "GPS jitter" that can be useful when ultra stable short term performance is needed.

The ASCII output continues to provide data as before so that the "open-loop" GPS-VCXO phase drift can be monitored.

NOTE: In this equipment switches S1/2/3 are also paralleled by a thumbwheel switch on the front panel. Thus if you want to use S1/2/3 directly, the panel switch must be placed to "7". Normally though, you will use the panel switch, so S1/2/3 (and 6/7/8) must be set to open / off / logic high.

ASCII Output

Format: 9600 baud 8N1

At each 30 second DAC update, the controller prints three five-digit numbers (e.g. `00803 65392 00003`)

The first of the three numbers is the total count from the phase detector counter U2A/U4 for the previous 30 seconds. When multiplied by the constant 41.7 ns per count divided by 30 counting intervals = 1.39 ns, this number is the phase difference in nanoseconds between GPS and the VCXO. The controller attempts to keep this count constant at the value 800. By using a phase difference offset from zero the controller can easily track both positive and negative phase changes.

The second of the three ASCII numbers is the value the digital filter is currently sending to the DAC to control the VCXO frequency. This number can be either positive or negative depending on whether a positive or negative VCXO disciplining voltage is needed and is in two's complement binary notation. Values larger than 32768 are interpreted as negative and equal to the value minus 65536. Only the most significant 16 bits of the 18-bit DAC input are printed.

The third ASCII value indicates the status of the controller. This number is a combination of three values arranged so that it is easy to see the status at a glance.

The current filter switch setting determines the lowest decimal place (0-7).

If the phase has just changed abruptly, which invokes a de-glitching algorithm in the software, the value 10 is added

If the phase difference is far from the set point, suggesting that the PLL is not locked, the value 100 is added to the number.

For example, the value 105 indicates that the filter time constant 5 is in use and that the phase lock may be questionable.

JRM

Original: 2003 Feb 13
Rev 2: 2005 Dec 16 - Page 4: enclosure specified; Navman URL updated
Rev 3: 2017 Mar 01 - References, diagrams, text and URLs updated
Rev 4: 2020 July 19 - Page 4: URLs updated